ABSTRACT

EQUALIZER ARCHITECTURE

An equalizer is divided between two tapped delay lines. One half of the sampled data is passed along one delay line, and the other half of the sampled data is passed along the other delay line. Delayed samples are passed to two summing circuits, and the output is formed from the two summing circuits alternately. This structure has the advantage that, by doubling the number of components, each component effectively only needs to operate at half the rate which would be required in a conventional structure. This allows the equalizer to operate successfully with signals at higher data rates.